GTTEST

The main purpose of GTTEST is to verify that the **Guide Technology Counter** in the PC is operational. This "GT" Counter is used to do the Verifications and Calibrations for the PTG, PE Deskew, and PE Strobes.

THEORY

To do the test, the counter needs a waveform from the Q2/62. The signal TG0 (Timing Generator 0) is brought out on the CSC40 Load Board to the two Probe Connectors on the front. These two connectors are shorted together so the same signal appears on both connectors.

The TG0 signal was chosen because it was easily available on the load board, although any of the TG's in the Q2 could have been used.

The GTTEST consists of triggering (starting) the counter on one edge of the TG0 signal and stopping the counter on the next opposite edge. The measured value of the counter is then compared to be within the limits of the expected value stored in the program.

DETAILS

The START probe is used to Trigger (Start) the counter and the STOP probe ends the measurement. The test is done in **3 tests** with each of the tests triggered at a different voltage level.

Each of the 3 tests measures the time from the rising edge to the falling edge and then repeats the measurement using the reverse transitions. See following table:

Test #	Trigger Voltage	Start Edge	Stop Edge	LOW Limit	HIGH Limit
1a	1.0V	Rising	Falling	38ns	53ns
1b	1.0V	Falling	Rising	47ns	60ns
2a	1.5V	Rising	Falling	43ns	56ns
2b	1.5V	Falling	Rising	44ns	57ns
3a	2.0V	Rising	Falling	46ns	59ns
3b	2.0V	Falling	Rising	40ns	53ns

TG0 is programmed to be a **100ns** cycle time square wave with **50ns** levels. That is, from its rising edge to its falling edge is **50ns** and likewise, from its falling edge to its rising edge is also 50ns. The counter is used to measure each of these 50ns values. However, since the start and stop is triggered at "non-midpoints", the actual time measured will be different than expected.

If the measured value is outside of these LOW / HIGH ranges, a **FAILURE** is set.

An additional test is performed after each of the three tests to verify the Q2 is indeed producing a **100ns cycle time**. The two measurements are added together ideally equaling 100ns. The test is set to PASS within the following limits:

Added Measure Values	Total	LOW Limit	HIGH Limit
Rise to Fall + Fall to Rise	= 100ns	97ns	103ns

GTTIMES

The purpose of GTTIMES is to provide a visual record of the values measured using the GTTEST program.

THEORY

When GTTEST is executed, each test takes two measurements. These are the measured time from the Rising Edge to the Falling Edge and from the Falling Edge to the Rising Edge of TG0.

DETAILS

The 1ST measured value, rise to fall, is stored in the register **LOWER**, the 2nd measurement, fall to rise, is stored in the register **UPPER**. These are displayed in nanoseconds.

These two values are then added and displayed as "**TOTAL**". This is repeated for all three tests and voltage levels.

FAILURES

A TEST with a measured value outside the set ranges will have a FAILURE displayed. Typical failures would include:

- ➔ Bad GT Counter or Probes
- ➔ Bad PTG (typically the Analog Board)
- ➔ Bad 74ABT125 on CSC40 Board or bad Probe Connectors
- ➔ Less likely: Q2 Front Panel, Mother Board, ZIF Connector (Ld Bd or PTG)

IF NO values measured, long timeouts in measurements: Check all connections, look at probes and connectors, reseat PTG, reseat CSC40, verify with scope, signals are coming to TP on CSC40.
IF values measured, but way out of range: Check the 74ABT125, try another CSC40, reseat probes and move cables away from AC lines, try another PTG (if all else OK, probably is PTG)
IF values measured, but slightly out of range: Let Q2 warm up more, try tests again, reseat PTG, reseat CSC40, reseat Probes, change the 74ABT125 on CSC40, try another CSC40 – possibly PTG.

SAMPLE DISPLAY

```
LOWER = START Rising to STOP Falling  -  UPPER = START Falling to STOP Rising
============================================================================
Test 1 @ 1V Trigger - Lower Limit= 38ns to 53ns - Upper= Limit 47ns to 60 ns
LOWER      =          50
UPPER      =          49
TOTAL Cycle Time - Should be 100ns - PASS is between  97ns <==> 103ns
TOTAL      =          99
PASSED

Test 2 @ 1.5V Trigger - Lower Limit= 43ns to 56ns - Upper= Limit 44ns to 57ns
LOWER      =          50
UPPER      =          49
TOTAL Cycle Time - Should be 100ns - PASS is between  97ns <==> 103ns
TOTAL      =          99
PASSED

Test 3 @ 2.0V Trigger - Lower Limit= 46ns to 59ns - Upper= Limit 40ns to 53ns
LOWER      =          52
UPPER      =          47
TOTAL Cycle Time - Should be 100ns - PASS is between  97ns <==> 103ns
TOTAL      =          99
FAILED
Offset set to -0.292 nanoseconds
```